**GBN Govt. Polytechnic Nilokheri, Karnal**

**Electrical Engineering Department**

**Lesson plan**

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| **Name of Faculty** | Sh. Ajay Kishor |
| **Discipline** | Electrical Engineering |
| **Semester** | 4th |
| **Subject** | Digital Electronics |
| **Lesson Plan Duration** | 16Week(From March 2023 to June 2023)Theory-04,Practical -02 |
| **Work load [Theory + Practical] Per Week** | Sh. Ajay Kishor |

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|  | **Topic(Including Assignment/Test)** | | **Practical**  **day** | | **Topic** | |
| 1st | **1:NumberSystems** | | Day1 | | Verification and interpretation of truth table for AND,OR, | |
| Decimal, binary | |
| Octal and hexadecimal number systems | |
| And the irinter-conversion | |
| 2nd | Numerical based on inter-conversion | | Day2 | | NOT,NAND,NOR,X-OR gates | |
| Binary and Hexa decimal addition | |
| Subtraction and multiplication | |
| 1’sandmethodsofaddition/subtraction | |
| 3rd | 2’scomplement | | Day3 | | Revision and checking | |
| Numerical/ problems | |
| Numerical/ problems | |
| **2:Gates**;Definition,symbolandtruthtablesforinverter,OR, | |
| 4th | AND, NAND | | Day4 | | Construction of Half Adder  Using gates | |
| NOR and X-OR and | |
| Equivalence circuit(Ex-NOR) | |
| Revision/assignment | |
| 5th | Class test | | Day5 | | Construction of Full Adder using gates | |
| **3:Boolean Algebra** ; Boolean Relations and their applications | |
| DeMorgan’s Theorems | |
| K-Map for two variables | |
| 6th | k-mapfor 4variable | | Day6 | | Revision and checking | |
| Numerical based onk-map | |
| Numerical based onk-map | |
| **4:CombinationalCircuits** | |
| 7th | Half adder with explanation | | Day7 | | To verify the truth table for JK flip-flop | |
| Full adder | |
| Encoder | |
| Decoder | |
| 8th | Multiplexer/Demultiplexer | | Day8 | | Revision and checking | |
| Display Devices(LED,LCD | |
| and7-segmentdisplay) | |
| Revision/assignment | |
| 9th | Class test | | Day9 | | Construction and testing of any counter | |
| **5:Flip-Flops;**J-KFlip-Flop | |
| R-S Flip-Flop | |
| D-TypeFlip-Flop | |
| 10th | T-TypeFlip-Flop | | Day10 | | Quiz and assessment | |
| ApplicationsofFlip-Flops | |
| Revision/assignment | |
|  | Class test |  | |  | |
| 11th | **6:IntroductionofShiftRegistersand**  **Counters** | Day1 | | Verification of operation of a8-bit D/A Converter | |
| With types |
| And Counters |
| With types |
| 12th | Revision/assignment |
| Class test | Day1 | | Revision and checking | |
| **7:A/D and D/A Converters** |
| A/D converter(Counter ramp |
| 13th | Successive approximation method of A/D  Conversion) | Day1 | | Revision and checking | |
| D/A converters(Binary weighted |
| R-2RD/A Converter) |
| Revision/assignment |
| 14th | Class test | Day1 | | Quiz and revision | |
| **8:Semi-conductorMemories** |
| With its Types |
| Merits ,demerits, |
| 15th | And applications | Day1 | | Revision and checking | |
| Revision/assignment |
| 16th | Class test | Day1 | | Revision and checking | |
| Revision/Review/Test of old HSBTE Papers |